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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,422	10/20/2003	Robert Kaiser	W&B-INF-1960	2803

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EXAMINER	
ASSESSOR, BRIAN J	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,422	KAISER ET AL.	
	Examiner	Art Unit	
	Brian J. Assessor	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Deas (6,041,422).

As per claim 1:

In a semiconductor memory module divided into banks and having an address structure in which each address is associated with a bank organized in rows and columns and defined with a row address, a column address, and a bank address, a method for comparing a memory access address with a known address of a faulty memory cell, the method which comprises:

in a first cycle, activating one row using a row address and an associated bank address;

in a second cycle, accessing the activated row using a column address and a bank address;

during the activation of the row:

a) comparing the row address of the activated row with the row address of the faulty memory cell, and passing a comparison result to a latching circuit (Deas column 4, lines 26-27) outputting an output signal to a logic stage; (Deas column 5, lines 47-51; column 6, lines 64-66; the comparator takes row address from the address bus and sends it to the next logic state.)

b) comparing the bank address with the bank address of the faulty memory cell passing a bank address comparison result to the logic stage; (Deas column 5, lines 47-51; column 6, lines 57-61; the comparator takes row address from the address bus and sends it to the next logic state.)

c) comparing the column address with the column address of the faulty memory cell and passing the comparison result to the logic stage; (Deas column 5, lines 47-51; column 6, lines 64-66; the comparator takes row address from the address bus and sends it to the next logic state.)

d) obtaining an activation pulse from a rising flank of a bank selection signal in a pulse generator and passing the activation pulse to the latching circuit if the bank address comparison result indicates a match and an enable register is set; (Deas column 4, lines 22-26; clock cycles are used to change the states of the comparison process.)

e) outputting a latching signal with the latching circuit if the comparison result in step a) is positive and an activation pulse has arrived from step d); (Deas column 4, lines 22-26; clock cycles are used to change the states of the comparison process.)

outputting a hit signal with the logic stage, the hit signal indicating access to a faulty memory cell, if the comparison results in steps b) and c) are positive and the latching circuit is outputting the latching signal. (Deas column 5, lines 53-57; the results of the comparison are positive and creates an enable signal if the comparison of the two addresses are identical.)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Assessor whose telephone number is (571) 272-0825. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BA

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